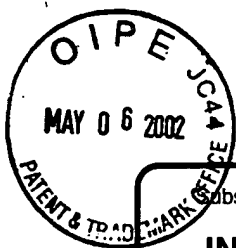


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		Filing Date	August 15, 2001		
		First Named Inventor	Reto Stamm		
		Art Unit	2819		
		Examiner Name	Unknown		
Sheet	2	of	2	Attorney Docket Number	X-727 US

OTHER – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
BT		Xilinx, Inc.; "The Programmable Logic Data Book"; September 1996; available from Xilinx, Inc., 2100 Logic Drive, San Jose, California 95124; pp. 4-251 to 4-286.	
BT		Eric Lechner and Steven A. Guccione; "The Java Environment for Reconfigurable Computing"; Proceedings - Field Programmable Logic and Applications, 7th International Workshop, FPL 1997; LONDON, UK; September 1-3, 1997, pp. 284-293.	
BT		Iseli et al.; "A C++ Compiler for FPGA Custom Execution Units Synthesis"; April 19-21, 1995; IEEE Symposium on FPGAs for Custom Computing Machines; pp. 173-179.	
BT		Peterson et al.; "Scheduling and Partitioning ANSI-C Programs Onto Multi-FPGA CCM Architectures"; IEEE Symposium on FPGAs for Custom Computing Machines; April 17-19, 1996; pp. 178-187.	
BT		Guccione et al.; "A Data-Parallel Programming Model for Reconfigurable Architectures"; April 5-7, 1993; IEEE Workshop on FPGAs for Custom Computing Machines; pp. 79-87.	

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